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EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 07/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10-057,707	Zhang et al.
	Examiner	Group Art Unit
	SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-23 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-23 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

DETAILED ACTION

Specification

Claims 2, 9, 13 and 20 are objected to because of the following informalities: In claim 2, this claim depends upon itself. Since it is the second claim as originally filed it is clear to the examiner that the dependency should have been that of claim 1 instead of claim 2. Accordingly, it will be assumed that claim 2 is actually dependent on claim 1 for examining purposes. Claims 9, 13 and 20 all recite "the first device and the second device and n-channel CMOS devices". This appears to be a typographical error where the second "and" should be an "are". It will be assumed that "are" was meant in these claims for examining purposes. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Welland 6,233,441 (Welland).

Figures 2 and 3 of Welland disclose a method of tuning a voltage controlled oscillator (VCO) 212. The frequency of oscillation of the VCO is measured, i.e. ascertained, by the divider 214 in combination with the connection to the output of the VCO. This measured frequency of oscillation is compared via the phase detector to a desired frequency in the standard way in the phase locked loop of Welland. An analog logic signal VC is generated and applied to a resistor 310. The resistor 310 or "first isolation resistor" is coupled to a first capacitor 308 and a second capacitor 312 that happens to be a junction varactor (See column 7 around line 37). The signal VC is a control voltage and thus "the first isolation resistor is configured to recive a control voltage." The junction varactor is also a "first varactor

diode" that is coupled to the first capacitor as noted above. The first capacitor is coupled to the "first" inductor LEXT and the second capacitor is coupled to a first supply terminal that happens to be ground.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Welland 6,233,441 (Welland) in view of Gibilisco .

All the same reasoning as applied to claims 1, 2 and 4 above and the following: Welland states that only the circuitry within the dotted line shown in Figure 2 is integrated. Claims like claim 5 recites "an integrated circuit" and is not specific as to how many chips the circuit is to be integrated on. It is very well known to integrate a circuit on a single or on multiple chips. This as recognized by Gibilisco has the advantages of increased compactness, increased speed, and lower power requirements as compared to the same circuit being composed of discrete-component elements.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the circuitry of Welland on either a single chip or on multiple chips so as to increase compactness, increase speed and lower power requirements as taught by Gibilisco.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Welland 6,233,441 (Welland)

All the same reasoning as applied to claims 1, 2 and 4 above and the following: The varactor shown in Welland is a junction varactor. Welland does not show a MOS varactor. However, it is well known that a MOS varactor is an art recognized equivalent to the junction varactor. The examiner takes Official Notice of this fact. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute a MOS varactor for the varactor of Welland since the examiner takes Official Notice of the equivalence of the junction varactor and the MOS varactor for their

use in the electronic art and the selection of any of these known equivalents to forms a variable capacitance would be within the level of ordinary skill in the art.

Claims 5-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strom 6,239,665 (Strom) in view of Kenyon 3,784,917 and Gibilisco "Handbook of Radio and Wireless Technology" (Gibilisco).

Figure 1A of Strom discloses a voltage controlled oscillator (VCO). Note that the control voltage VC of Strom varies the frequency of the oscillator and thus the oscillator of Strom is clearly a VCO (See column 3, around line 42.). Figure 1A of Strom clearly shows the first inductor 108, the second inductor 110, the first capacitor 114, the second capacitor 116, the first device, i.e. n-channel FET 126, the second device, i.e. n-channel FET 128 and the common source current source 130. Note that there are P-channel devices like element 104 and thus to integrate the arrangement as noted below would result in an obvious consequence of having the integrated circuit being a CMOS device, i.e. one that contains both n and p channel devices. The first capacitor is coupled to the first inductor as is clearly illustrated. The second capacitor is coupled to the first inductor through inductor 110 as is clearly illustrated. Figure 1A clearly illustrates the first device having a drain coupled to the first inductor and a gate coupled to the second inductor. Figure 1A clearly illustrates the second device having a drain coupled to the second inductor and a gate coupled to the first inductor. Elements 114 and 132 in combination merely form a variable capacitance element that is controlled by an analog logic signal SO. This helps tunes the oscillator to a desired range. Likewise elements 116 and 134 in combination merely form a variable capacitance element in the other leg of the oscillator that controlled by the same analog logic signal SO. This too helps tune the oscillator to a desired range. The two variable capacitances clearly work in combination with each other. Note that these variable capacitances are connected between the inductive element(s) of the oscillator and ground in Strom. Strom is silent on integrating the circuit. Strom also lacks the use of the two varactor diodes or MOS varactors, i.e. third and fourth capacitors, connected in series with the first and second capacitors respectfully that makes up in effect two variable capacitances. Note that Strom has two variable capacitance elements that are composed of at least elements 114, 116, 138 and 134. Strom also lacks the isolation resistors one connected between the first and third capacitors and the other connected between the second and fourth capacitors. Kenyon discloses that a variable capacitance 12 composed of two capacitor elements connected in series between the inductive element of the oscillator and the ground is an equivalent structure known in the art. Note that the capacitive element that is connected directly to ground in Kenyon is a varactor diode. This is also a well-known structure to tune the oscillator (See column 3, around line 18 of Kenyon.). The center nodes of the series circuit of Kenyon is connected an isolation resistor 13 which in turn is connected to the analog logic signal that is used to

control the range of the oscillator i.e. it is tuned to a particular range. Strom is silent on using the VCO circuit in a RF transceiver .

Therefore because these two variable capacitances were art-recognized equivalents in the oscillator art at the time the invention was made, one of ordinary skill in the art at the time the invention was made would have found it obvious to substitute a variable capacitance element composed of a series arrangement of two capacitors with at least one of the capacitors being a varactor diode connected to ground and includes an isolation resistor connected to the center node of this series arrangement that connects the variable capacitance to a control voltage for each of the variable capacitance arrangements (114, 116, 138, 134) of Strom.

Gibilisco discloses that it is very well known to integrate a circuit on a single or on multiple chips. This as recognized by Gilisco has the advantages of increased compactness, increased speed, and lower power requirements as compared to the same circuit being composed of discrete-component elements.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the circuitry of Strom and Kenyon so as to increase speed and lower power requirements as taught by Gibilisco.

It is well known that a MOS varactor is an art recognized equivalent to the junction varactor. The examiner takes Official Notice of this fact. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute a MOS varactor for the varactor of Welland given the art recognized equivalence.

It is well known in the art that RF transceivers commonly employ conventional VCO's especially for tuning. The arrangement as made obvious above is a conventional VCO arrangement. Accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the VCO arrangement made obvious above in a RF transceiver employing conventional VCOs for the VCO employed therein, because as the RF transciever teaches to employ a conventional VCO any art recognized equivalent VCO would have been usable such as the conventional VCO made obvious above

Claims 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyashita et al. 4,673,892 (Miyashita) in view of Strom 6,239,665 (Strom) in further view of Gibilisco and Kenyon 3,784,917 (Kenyon).

Figure 1 of Miyashita discloses the generic phase locked loop (PLL) as claimed having a phase detector 28 configured to receive a reference clock 24, 26, a low pass filter 18 coupled to the phase detector 28 and voltage controlled oscillator (VCO) 20 coupled to the low pass filter and a divider 22 coupled "between" the VCO and the low pass filter. Note that in applicant's invention the divider 140 is coupled between the phase detector 110 and the VCO 130 which according to applicant makes this divider 140 coupled "between" the VCO 130 and the low pass filter 120 as meant by applicant. Figure 1 of Miyashita clearly shows the same structure. Miyashita, however, is silent on the specific structure that makes up the VCO.

The specific VCO structure claimed in claims 19-23 is the same VCO structure as is claimed claims 5-18. As noted above this structure would have been obvious to one of ordinary skill in the art and in the interest of being concise applicant is referred to the above reasoning presented in the rejection of claims 5-18 rejecting this VCO structure as having been obvious to one of ordinary skill in the art because the same reasoning applies here.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the VCO made obvious under Strom, Gibilsco and Kenyon in place of the VCO of Miyashita because, as the reference is silent as to the specifics of the VCO, any art-recognized equivalent VCO would have been usable such as the VCO structure made obvious under Strom, Gibilisco and Kenyon.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cao 6,542,043 discloses a VCO with "cross coupled gates" (See Figure 4). Koyama et al. 01208902 and Rogers et al. "The effect of varactor nonlinearity on the phase noise of completely integrated VCO's" both disclose various VCO structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:00 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
May 20, 2003

Michael B. Shingleton

MICHAEL B. SHINGLETON
PRIMARY EXAMINER
GROUP